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Design and Test Technology for Dependable Systems-on-chip - Raimund Ubar 2011-01-01
"This book covers aspects of system design and efficient modelling, and also introduces various fault models and fault mechanisms associated with digital circuits integrated into System on Chip (SoC), Multi-Processor System-on Chip (MPSoC) or Network on Chip (NoC)"--
Proceedings of the ... Midwest Symposium on Circuits and Systems - 1999

On-Chip Current Sensors for Reliable, Secure, and Low-Power Integrated Circuits - Rodrigo Possamai Bastos 2019-09-30
This book provides readers with insight into an alternative approach for enhancing the reliability, security, and low power features of integrated circuit designs, related to transient faults, hardware Trojans, and power consumption. The authors explain how the addition of integrated sensors enables the detection of ionizing particles and how this information can be processed at a high layer. The discussion also includes a variety of applications, such as the detection of hardware Trojans and fault attacks, and how sensors can operate to provide different body bias levels and reduce power costs. Readers can benefit from these sensors-based approaches through designs with fast response time, non-intrusive integration on gate-level and reasonable design costs.
Advanced Hydroinformatic Techniques for the Simulation and Analysis of Water Supply and Distribution Systems - Manuel Herrera 2018-07-19
This book is a printed edition of the Special Issue "Advanced Hydroinformatic Techniques for the Simulation and Analysis of Water Supply and Distribution Systems" that was published in Water
Proceedings - 2003

Analog Circuit Design - Johan Huijsing 1995-12-31
Johan H. Huijsing This book contains 18 tutorial papers concentrated on 3 topics, each topic being covered by 6 papers. The topics are: Low-Noise, Low-Power, Low-Voltage Mixed-Mode Design with CAD Tools Voltage, Current, and Time References The papers of this book were written by top experts in the field, currently working at leading European and American universities and companies. These papers are the reviewed versions of the papers presented at the Workshop on Advances in Analog Circuit Design. which was held in Villach, Austria, 26-28 April 1995. The chairman of the Workshop was Dr. Franz Dielacher from Siemens, Austria. The program committee existed of Johan H. Huijsing from the Delft University of Technology, Prof.Willy Sansen from the Catholic University of Leuven, and Dr. Rudy 1. van der Plassche from Philips Eindhoven. This book is the fourth of aseries dedicated to the design of analog circuits. The topics which were covered earlier were: Operational Amplifiers Analog to Digital Converters Analog Computer Aided Design Mixed AlD Circuit Design Sensor Interface Circuits Communication Circuits Low-Power, Low-Voltage Integrated Filters Smart Power As the Workshop will be continued year by year, a valuable series of topics will be built up from all the important areas of analog circuit design. I hope that this book will help designers of analog circuits to improve their work and to speed it up.
Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors - José Rodrigo Azambuja 2014-07-07
This book describes fault tolerance techniques based on software and hardware to create hybrid techniques. They are able to reduce overall performance degradation and increase error detection when associated with applications implemented in embedded processors. Coverage begins with an extensive discussion of the current state-of-the-art in fault tolerance techniques. The authors then discuss the best trade-off between software-based and hardware-based techniques and introduce novel hybrid techniques. Proposed techniques increase existing fault detection rates up to 100%, while maintaining low performance overheads in area and application execution time.
ESD Design and Analysis Handbook - James E. Vinson 2012-12-06
Electrostatic Discharge is a pervasive issue in the semiconductor industry affecting both manufacturers and users of semiconductors. This easy-to-read, practical handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students, engineers, circuit designers and failure analysts.
Unifying Electrical Engineering and Electronics Engineering - Song Xing 2013-08-24
Unifying Electrical Engineering and Electronics Engineering is based on the Proceedings of the 2012 International Conference on Electrical and Electronics Engineering (ICEE 2012). This book collects the peer reviewed papers presented at the conference. The aim of the conference is to unify the two areas of Electrical and Electronics Engineering. The book examines trends and techniques in the field as well as theories and applications. The editors have chosen to include the following topics; biotechnology, power engineering, superconductivity circuits, antennas technology, system architectures and telecommunication.
Microelectronics Failure Analysis - 2004-01-01
For newcomers cast into the waters to sink or swim as well as seasoned professionals who want authoritative guidance desk-side, this hefty volume updates the previous (1999) edition. It contains the work of expert contributors who rallied to the job in response to a committee's call for help (the committee was assigned to the update by the Electron
Emerging Technologies in NDT - D. Hemelrijck 2003-01-01
This is the third volume of a series of proceedings including papers presented at the respective International Conferences entitled: "Emerging Technologies in Non-Destructive Testing (NDT)" that have been held in Greece since 1995. This volume contains papers presented at the third Conference on Emerging Technologies in Non-Destructive Testing (NDT) Conference, convened at Thessaloniki, Greece in 2003. Papers cover a range of subjects including: * interdisciplinary efforts to gain maximum benefit from capabilities from other science and engineering fields * integration of several methods to form multimode systems for improved reliability * increased use of computer simulation to investigate the response of specific methods This work also covers improvements, enhancements and new and innovative ideas in NDT and should be of interest to engineers, researchers, quality control managers, as well as teachers and graduate students in the field.
Testing and Measurement: Techniques and Applications - Kennis Chan 2015-06-11
Testing and Measurement: Techniques and Applications is divided into 6 sections: Microwave, Ultrasonic and Acoustic Measurement and Application; Material Performance and Measuring and Testing Technique; Laser, Optics Fiber and Sensor; Industrial Autoimmunization and Measurement; Artificial Intelligence and

Application; and Image, Signal and In

Leakage in Nanometer CMOS Technologies - Siva G. Narendra 2006-03-10

Covers in detail promising solutions at the device, circuit, and architecture levels of abstraction after first explaining the sensitivity of the various MOS leakage sources to these conditions from the first principles. Also treated are the resulting effects so the reader understands the effectiveness of leakage power reduction solutions under these different conditions. Case studies supply real-world examples that reap the benefits of leakage power reduction solutions as the book highlights different device design choices that exist to mitigate increases in the leakage components as technology scales.

Proceedings of the ... International Conference on Microelectronics - 2002

On-Line Testing for VLSI - Michael Nicolaidis 2013-03-09

Test functions (fault detection, diagnosis, error correction, repair, etc.) that are applied concurrently while the system continues its intended function are defined as on-line testing. In its expanded scope, on-line testing includes the design of concurrent error checking subsystems that can be themselves self-checking, fail-safe systems that continue to function correctly even after an error occurs, reliability monitoring, and self-test and fault-tolerant designs. On-Line Testing for VLSI contains a selected set of articles that discuss many of the modern aspects of on-line testing as faced today. The contributions are largely derived from recent IEEE International On-Line Testing Workshops. Guest editors Michael Nicolaidis, Yervant Zorian and Dhiraj Pradhan organized the articles into six chapters. In the first chapter the editors introduce a large number of approaches with an expanded bibliography in which some references date back to the sixties. On-Line Testing for VLSI is an edited volume of original research comprising invited contributions by leading researchers.

ISCAS 2001 - 2001

CMOS Electronics - Jaume Segura 2004-03-26

CMOS manufacturing environments are surrounded with symptoms that can indicate serious test, design, or reliability problems, which, in turn, can affect the financial as well as the engineering bottom line. This book educates readers, including non-engineers involved in CMOS manufacture, to identify and remedy these causes. This book instills the electronic knowledge that affects not just design but other important areas of manufacturing such as test, reliability, failure analysis, yield-quality issues, and problems. Designed specifically for the many non-electronic engineers employed in the semiconductor industry who need to reliably manufacture chips at a high rate in large quantities, this is a practical guide to how CMOS electronics work, how failures occur, and how to diagnose and avoid them. Key features: Builds a grasp of the basic electronics of CMOS integrated circuits and then leads the reader further to understand the mechanisms of failure. Unique descriptions of circuit failure mechanisms, some found previously only in research papers and others new to this publication. Targeted to the CMOS industry (or students headed there) and not a generic introduction to the broader field of electronics. Examples, exercises, and problems are provided to support the self-instruction of the reader.

Models in Hardware Testing - Hans-Joachim Wunderlich 2009-11-12

Model based testing is the most powerful technique for testing hardware and software systems. Models in Hardware Testing describes the use of models at all the levels of hardware testing. The relevant fault models for nanoscaled CMOS technology are introduced, and their implications on fault simulation, automatic test pattern generation, fault diagnosis, memory testing and power aware testing are discussed. Models and the corresponding algorithms are considered with respect to the most recent state of the art, and they are put into a historical context by a concluding chapter on the use of physical fault models in fault tolerance.

Nanometer Technology Designs - Nisar Ahmed 2010-02-26

Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges. Supply noise effects on chip performance, high test pattern volume, small delay defect test pattern generation, high cost of test implementation and application, and utilizing low-cost testers are among these challenges. This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test.

DCIS2002 - Salvador Bracho del Pino 2002

Este libro contiene las presentaciones de la XVII Conferencia de Diseño de Circuitos y Sistemas Integrados celebrado en el Palacio de la Magdalena, Santander, en noviembre de 2002. Esta Conferencia ha alcanzado un alto nivel de calidad, como consecuencia de su tradición y madurez, que lo convierte en uno de los acontecimientos más importantes para los circuitos de microelectrónica y la comunidad de diseño de sistemas en el sur de Europa. Desde su origen tiene una gran contribución de Universidades españolas, aunque hoy los autores participan desde catorce países

19th IEEE VLSI Test Symposium - 2001

Collects 58 papers from the April/May 2001 symposium that explore new approaches in the testing of electronic circuits and systems. Key areas in testing are discussed, such as BIST, analog measurement, fault tolerance, diagnosis methods, scan chain design, memory test and diagnosis, and test data compression and compaction. Also on the program are sessions on emerging areas that are gaining prominence, including low power testing, testing high speed circuits on low cost testers, processor based self test techniques, and core- based system-on-chip testing. Some of the topics are robust and low cost BIST architectures for sequential fault testing in datapath multipliers, a method for measuring the cycle-to-cycle period jitter of high-frequency clock signals, fault equivalence identification using redundancy information and static and dynamic extraction, and test scheduling for minimal energy consumption under power constraints. No subject index. c. Book News Inc.

Emerging Trends in Technological Innovation - Luis M. Camarinha-Matos 2010-02-26

Identifying Emerging Trends in Technological Innovation Doctoral programs in science and engineering are important sources of innovative ideas and techniques that might lead to new products and technological innovation. Certainly most PhD students are not experienced researchers and are in the process of learning how to do research. Nevertheless, a number of empiric studies also show that a high number of technological innovation ideas are produced in the early careers of researchers. The combination of the eagerness to try new approaches and directions of young doctoral students with the experience and broad knowledge of their supervisors is likely to result in an important pool of innovation potential. The DoCEIS doctoral conference on Computing, Electrical and Industrial En- neering aims at creating a space for sharing and discussing ideas and results from doctoral research in these inter-related areas of engineering. Innovative ideas and hypotheses can be better enhanced when presented and discussed in an encouraging and open environment. DoCEIS aims to provide such an environment, releasing PhD students from the pressure of presenting their propositions in more formal contexts.

Principles of Testing Electronic Systems - Samiha Mourad 2000-07-25

A pragmatic approach to testing electronic systems As we move ahead in the electronic age, rapid changes in technology pose an ever-increasing number of challenges in testing electronic products. Many practicing engineers are involved in this arena, but few have a chance to study the field in a systematic way-learning takes place on the job. By covering the fundamental disciplines in detail, Principles of Testing Electronic Systems provides design engineers with the much-needed knowledge base. Divided into five major parts, this highly useful reference relates design and tests to the development of reliable electronic products; shows the main vehicles for design verification; examines designs that facilitate testing; and investigates how testing is applied to random logic, memories, FPGAs, and microprocessors. Finally, the last part offers coverage of advanced test solutions for today's very deep submicron designs. The authors take a phenomenological approach to the subject matter while providing readers with

plenty of opportunities to explore the foundation in detail. Special features include: * An explanation of where a test belongs in the design flow * Detailed discussion of scan-path and ordering of scan-chains * BIST solutions for embedded logic and memory blocks * Test methodologies for FPGAs * A chapter on testing system on a chip * Numerous references

Contactless VLSI Measurement and Testing Techniques - Selahattin Sayil 2017-11-16
This book provides readers with a comprehensive overview of the state-of-the-art in optical contactless probing approaches, in order to fill a gap in the literature on VLSI Testing. The author highlights the inherent difficulties encountered with the mechanical probe and testability design approaches for functional and internal fault testing and shows how contactless testing might resolve many of the challenges associated with conventional mechanical wafer testing. The techniques described in this book address the increasing demands for internal access of the logic state of a node within a chip under test.

Proceedings, International Test Conference 1997 - 1997

Defect Oriented Testing for CMOS Analog and Digital Circuits - Manoj Sachdev 2013-06-29
Defect oriented testing is expected to play a significant role in coming generations of technology. Smaller feature sizes and larger die sizes will make ICs more sensitive to defects that can not be modeled by traditional fault modeling approaches. Furthermore, with increased level of integration, an IC may contain diverse building blocks. Such blocks include, digital logic, PLAs, volatile and non-volatile memories, and analog interfaces. For such diverse building blocks, traditional fault modeling and test approaches will become increasingly inadequate. Defect oriented testing methods have come a long way from a mere interesting academic exercise to a hard industrial reality. Many factors have contributed to its industrial acceptance. Traditional approaches of testing modern integrated circuits (ICs) have been found to be inadequate in terms of quality and economics of test. In a globally competitive semiconductor market place, overall product quality and economics have become very important objectives. In addition, electronic systems are becoming increasingly complex and demand components of highest possible quality. Testing, in general and, defect oriented testing, in particular, help in realizing these objectives. Defect Oriented Testing for CMOS Analog and Digital Circuits is the first book to provide a complete overview of the subject. It is essential reading for all design and test professionals as well as researchers and students working in the field. `A strength of this book is its breadth. Types of designs considered include analog and digital circuits, programmable logic arrays, and memories. Having a fault model does not automatically provide a test. Sometimes, design for testability hardware is necessary. Many design for testability ideas, supported by experimental evidence, are included.' ... from the Foreword by Vishwani D. Agrawal

Test Cost Reduction Techniques - Xiaoyun Sun 2005

Eddy-Current Characterization of Materials and Structures - George M. Free 1981-06

Interconnection Noise in VLSI Circuits - Francesc Moll 2004
This book addresses two main problems with interconnections at the chip and package level: crosstalk and simultaneous switching noise. Its orientation is towards giving general information rather than a compilation of practical cases. Each chapter contains a list of references for the topics.

IDDQ Testing of VLSI Circuits - Ravi K. Gulati 2012-12-06
Power supply current monitoring to detect CMOS IC defects during production testing quietly laid down its roots in the mid-1970s. Both Sandia Labs and RCA in the United States and Philips Labs in the Netherlands practiced this procedure on their CMOS ICs. At that time, this practice stemmed simply from an intuitive sense that CMOS ICs showing abnormal quiescent power supply current (IDDQ) contained defects. Later, this intuition was supported by data and analysis in the 1980s by Levi (RACD, Malaiya and Su (SUNY-Binghamton), Soden and Hawkins (Sandia Labs and the University of New Mexico), Jacomino and co-workers (Laboratoire d'Automatique de Grenoble), and Maly and co-workers (Carnegie Mellon University). Interest in IDDQ testing has advanced beyond the data reported in the 1980s and is now focused on applications and evaluations involving larger volumes of ICs that improve quality beyond what can be achieved by previous conventional means. In the conventional style of testing one attempts to propagate the logic states of the suspended nodes to primary outputs. This is done for all or most nodes of the circuit. For sequential circuits, in particular, the complexity of finding suitable tests is very high. In comparison, the IDDQ test does not observe the logic states, but measures the integrated current that leaks through all gates. In other words, it is like measuring a patient's temperature to determine the state of health. Despite perceived advantages, during the years that followed its initial announcements, skepticism about the practicality of IDDQ testing prevailed. The idea, however, provided a great opportunity to researchers. New results on test generation, fault simulation, design for testability, built-in self-test, and diagnosis for this style of testing have since been reported. After a decade of research, we are definitely closer to practice.

Mixed-Signal Circuits - Thomas Noulis 2018-09-03
Mixed-Signal Circuits offers a thoroughly modern treatment of integrated circuit design in the context of mixed-signal applications. Featuring chapters authored by leading experts from industry and academia, this book: Discusses signal integrity and large-scale simulation, verification, and testing Demonstrates advanced design techniques that enable digital circuits and sensitive analog circuits to coexist without any compromise Describes the process technology needed to address the performance challenges associated with developing complex mixed-signal circuits Deals with modeling topics, such as reliability, variability, and crosstalk, that define pre-silicon design methodology and trends, and are the focus of companies involved in wireless applications Develops methods to move analog into the digital domain quickly, minimizing and eliminating common trade-offs between performance, power consumption, simulation time, verification, size, and cost Details approaches for very low-power performances, high-speed interfaces, phase-locked loops (PLLs), voltage-controlled oscillators (VCOs), analog-to-digital converters (ADCs), and biomedical filters Delineates the respective parts of a full system-on-chip (SoC), from the digital parts to the baseband blocks, radio frequency (RF) circuitries, electrostatic-discharge (ESD) structures, and built-in self-test (BIST) architectures Mixed-Signal Circuits explores exciting opportunities in wireless communications and beyond. The book is a must for anyone involved in mixed-signal circuit design for future technologies.

Proceedings of the International Field Exploration and Development Conference 2020 - Jia'en Lin 2021-06-17
This book is a compilation of selected papers from the 10th International Field Exploration and Development Conference (IFEDC 2020). The proceedings focuses on Reservoir Surveillance and Management, Reservoir Evaluation and Dynamic Description, Reservoir Production Stimulation and EOR, Ultra-Tight Reservoir, Unconventional Oil and Gas Resources Technology, Oil and Gas Well Production Testing, Geomechanics. The conference not only provides a platform to exchanges experience, but also promotes the development of scientific research in oil & gas exploration and production. The main audience for the work includes reservoir engineer, geological engineer, enterprise managers senior engineers as well as professional students.

CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies - Andrei Pavlov 2008-06-01
The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

IEEE VLSI Test Symposium - 2005

Defect-Oriented Testing for Nano-Metric CMOS VLSI Circuits - Manoj Sachdev

2007-06-04
The 2nd edition of defect oriented testing has been extensively updated. New chapters on Functional, Parametric Defect Models and Inductive fault Analysis and Yield Engineering have been added to provide a link between defect sources and yield. The chapter on RAM testing has been updated with focus on parametric and SRAM stability testing. Similarly, newer material has been incorporated in digital fault modeling and analog testing chapters. The strength of Defect Oriented Testing for nano-Metric CMOS VLSIs lies in its industrial relevance.
Proceedings of Integrated Intelligence Enable Networks and Computing - Krishan Kant Singh Mer 2021-04-23
This book presents best selected research papers presented at the First International Conference on Integrated Intelligence Enable Networks and Computing (IIENC 2020), held from May 25 to May 27, 2020, at the Institute of Technology, Gopeshwar, India (Government Institute of Uttarakhand Government and affiliated to Uttarakhand Technical University). The book includes papers in the field of intelligent computing. The book covers the areas of machine learning and robotics, signal processing and Internet of things, big data and renewable energy sources.
Advances in Non Destructive Evaluation - Shyamsunder Mandayam
This book comprises the proceedings of the Conference and Exhibition on Non Destructive Evaluation (NDE 2020). The contents of the volume encompass a vast spectrum from Conventional to Advanced NDE including novel methods, instrumentation, sensors, procedures, and data analytics as applied to all industry segments for quality control, periodic maintenance, life estimation, structural integrity and related areas. This book will be a useful reference for students, researchers and practitioners.
The Electronic Design Automation Handbook - Dirk Jansen 2010-02-23
When I attended college we studied vacuum tubes in our junior year. At that time an average radio had ?ve vacuum tubes and better ones even seven. Then transistors appeared in 1960s. A good radio was judged to be one with more thententransistors. Latergoodradioshad15–20transistors and after that everyone stopped counting transistors. Today modern processors runing personal computers have over 10milliontransistorsandmoremillionswillbeaddedevery year. The difference between 20 and 20M is in complexity, methodology and business models. Designs with 20 tr- sistors are easily generated by design engineers without any tools, whilst designs with 20M transistors can not be done by humans in reasonable time without the help of Prof. Dr. Gajski demonstrates the Y-chart automation. This difference in complexity introduced a paradigm shift which required sophisticated methods and tools, and introduced design automation into design practice. By the decomposition of the design process into many tasks and abstraction levels the methodology of designing chips or systems has also evolved. Similarly, the business model has changed from vertical integration, in which one company did all the tasks from product speci?cation to manufacturing, to globally distributed, client server production in which most of the design and manufacturing tasks are outsourced.
Transient Electromagnetic-Thermal Nondestructive Testing - Yunze He 2017-05-25
Transient Electromagnetic-Thermal Nondestructive Testing: Pulsed Eddy Current and Transient Eddy Current Thermography covers three key areas of theories, methods and applications, primarily the multi-physics field, including eddy current, heat conduction and Infrared radiation for defect evaluation, lateral heat conduction, which is analyzed to detect parallel cracks, and longitudinal heat conduction, which is analyzed to detect depth defect, or that which is beyond skin depth. In addition, the book explores methods, such as time domain, frequency domain and logarithm domain, also comparing A-scan , B-scan and C-scan. Sections on defect identification, classification and quantification are covered, as are advanced algorithms, principal components analysis (PCA), independent components analysis (ICA) and support vector machine (SVM). The book uses a lot of experimental studies on multi-layer aluminum structures, honeycomb structure, CFRP in the aerospace field, and steel and coating in the marine rail and transportation fields. Presents two kinds of transient NDT testing, from theory and methodology, to applications Includes time domain frequency domain and logarithm domain, which are all analyzed Introduces A-scan , B-scan and C-scan, which are compared Provides experimental studies for real damages, including corrosion and blister in steel, stress in aluminum, impact and delamination in CFRP laminates and RCF cracks are abundant
IC Test Using the Energy Consumption Ratio - Wanli Jiang 2000